DON BOSCO INSTITUTE OF TECHNOLOGY, MUMBAI

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

Report on Alumni Talk by Mr. Hussain Neralwala

Topic: "How a chip is made: Conceptualization to Production"

Date: 7th August, 2020

Time: 5:00 - 6:00 p.m.

Venue: Zoom Meeting (Online Platform)

Speaker: Mr. Hussain Neralwala, Logic Design Head, GTCHE, Intel Bangalore

No of participants registered: 11

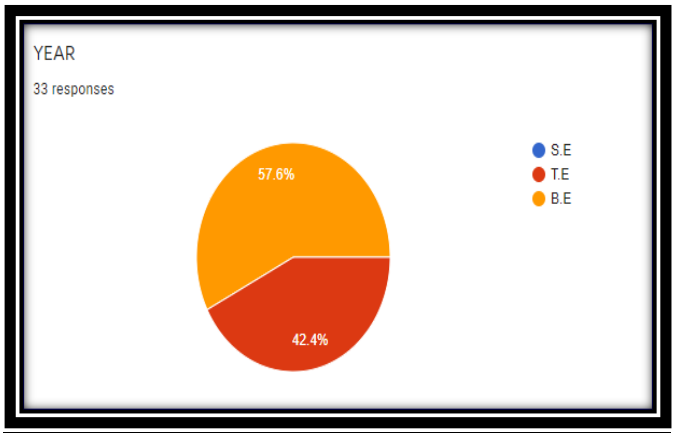
No of participants attended: 49

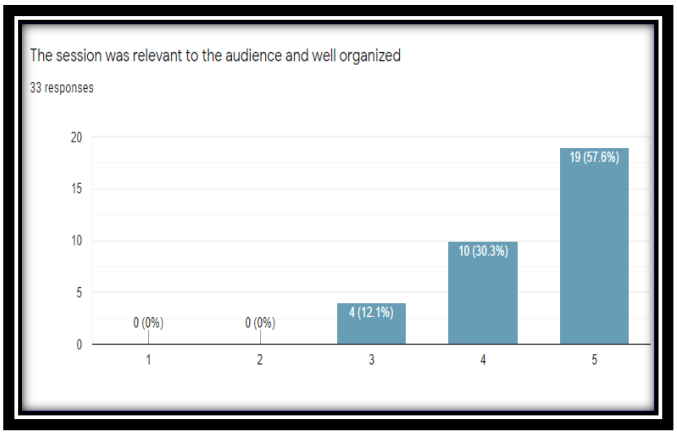
Description:

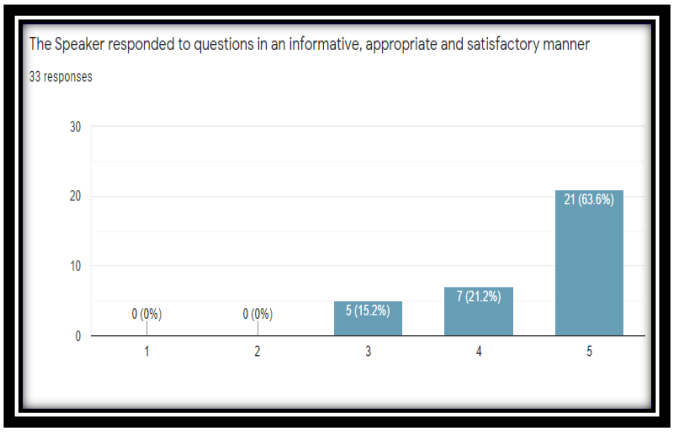
- The EXTC Department of DBIT organized an alumni talk on "How a chip is made: Conceptualization to Production" on the 7th August, 2020.
- The session commenced with Prof. Freda Carvalho of EXTC Department addressing the participants and welcoming the speaker for the talk.
- Prof. Freda Carvalho gave an introduction of the speaker, Mr. Hussain Neralwala, Logic Design Head, GTCHE, Intel Bangalore.
- Following the introduction, Mr. Hussain Neralwala took over and started the session by giving a brief introduction to his background in the field and his education.
- Further, he discussed about coupling of 'MOS transistor' with a brief introduction on 'Advent of VLSI'.
- Adding on he stated 'Moore's law' and how over the period of 1971-2018 it has evolved.
- He went on to further define the law, "Moore's law is the observation that the number of transistors in a dense integrated circuit doubles about every two years".
- All the participants learnt about how Moore's law is linked closely with processing speed and the pricing of the product.
- A brief explanation of SOC was given by the speaker by referring to the block diagram of the same.
- In the same vein, the sub-parts of SOC includes a central processing unit, memory, input/output ports and secondary storage – all on a single substrate or microchip, the size of a coin.

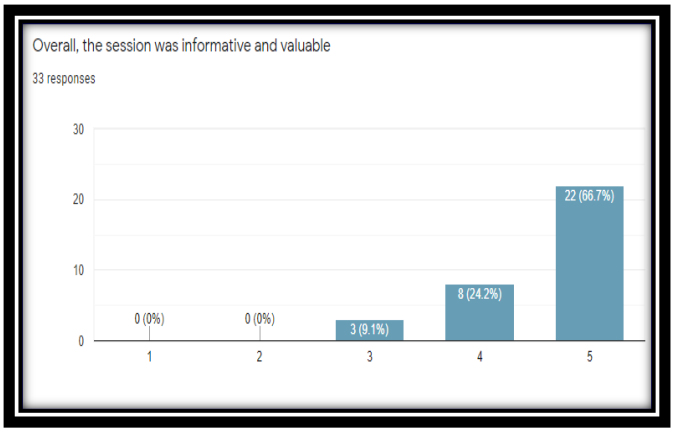
- In addition, he gave an idea of how one should follow the flow chart of steps during a specific ‘Design Flow’ of their component.
- He categorized the SOC Development team into 8 parts, namely- Architecture, Front-end, DFT, Validation, Emulation, Backend, Post-silicon and characterization.
- Moreover, he stressed on the trend of ‘Low Power Design’ and described about clock gating, power gating, dynamic voltage & frequency scaling (DVFS) and Hetero core.
- Concluding the talk, the session was opened to a Q&A round with the participants. The questions were selected from the participants from the zoom call and Mr. Hussain Neralwala addressed all of them very meticulously.
- The session was concluded with the vote of thanks delivered by Ms. Ajitha Rajkumar, Event Head, IEEE, EXTC Department after which the participants were requested to fill the feedback forms circulated on the WhatsApp groups.

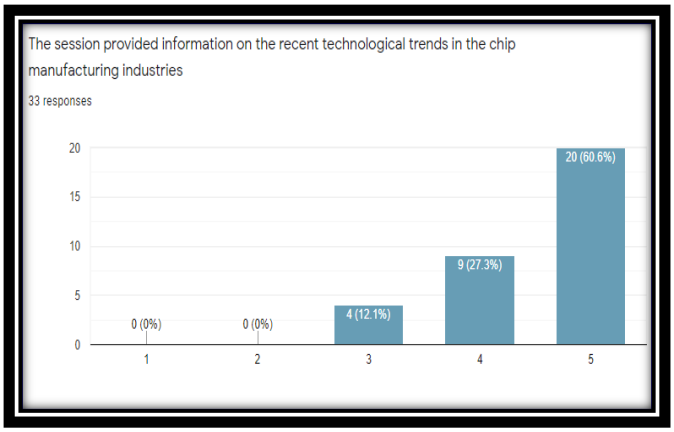
Feedback Analysis:

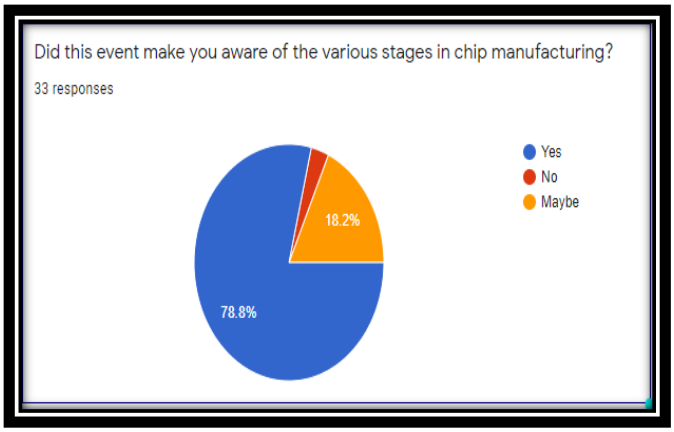


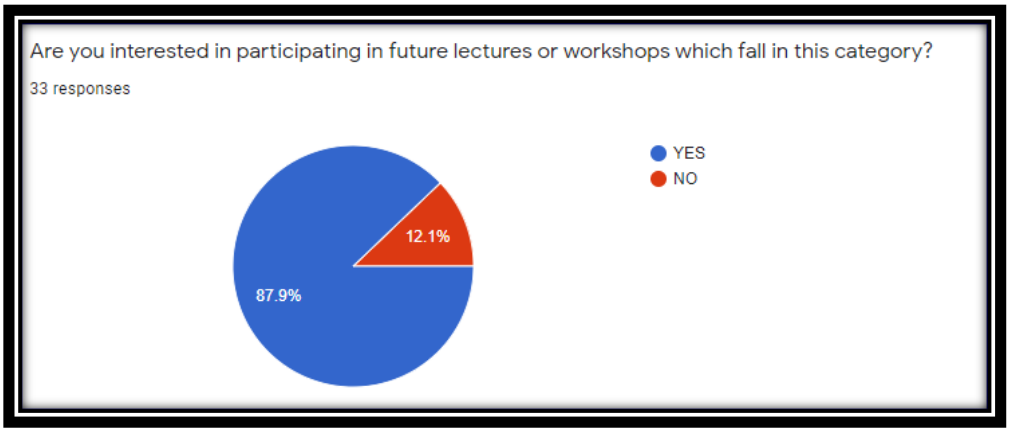








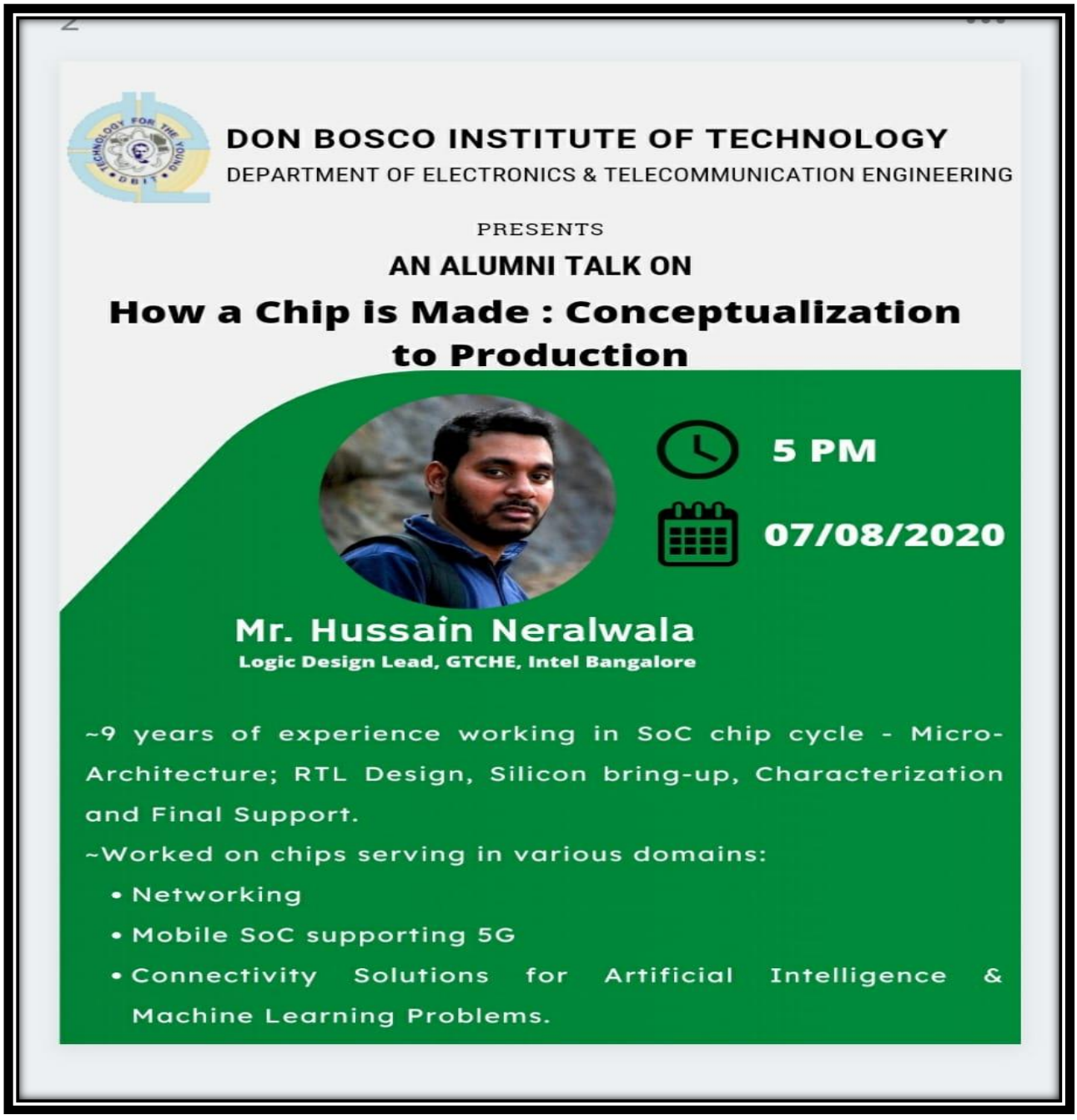




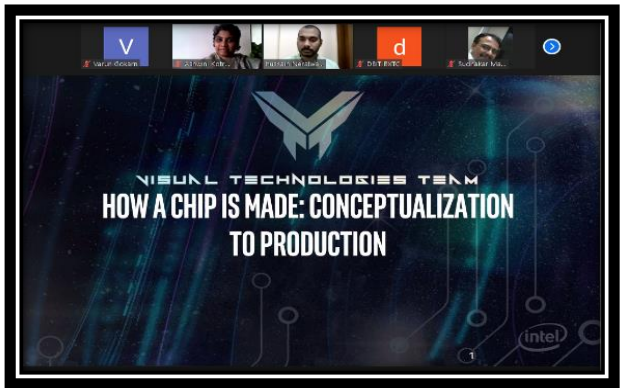
Summary of Webinar Analysis:

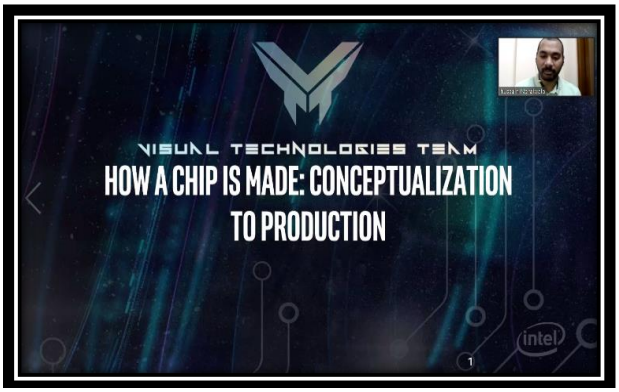
From the above analysis we can see the overall reception to the webinar was positive and the participants felt that the overall webinar was satisfactory and informative. As reflected by the feedback, the webinar helped many by gaining clear perspective on Chip production. A High number of the participants are interested in such future webinars.

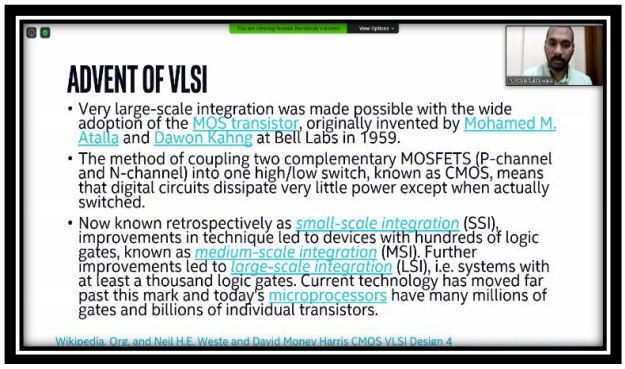
Event Poster:

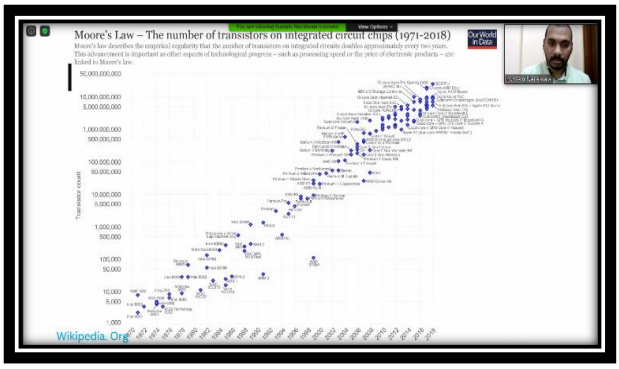


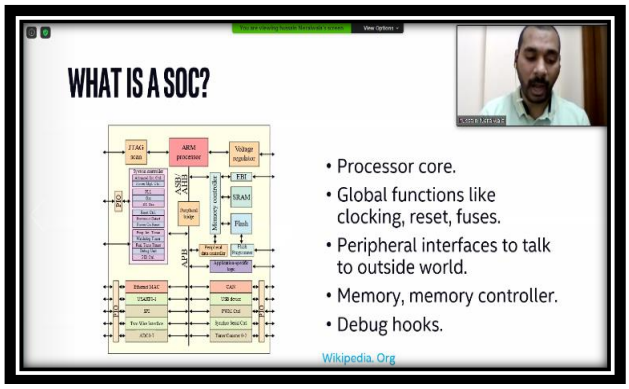
EVENT PICTURES:

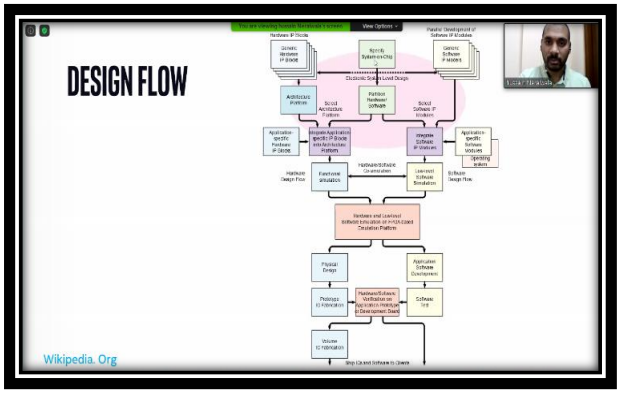


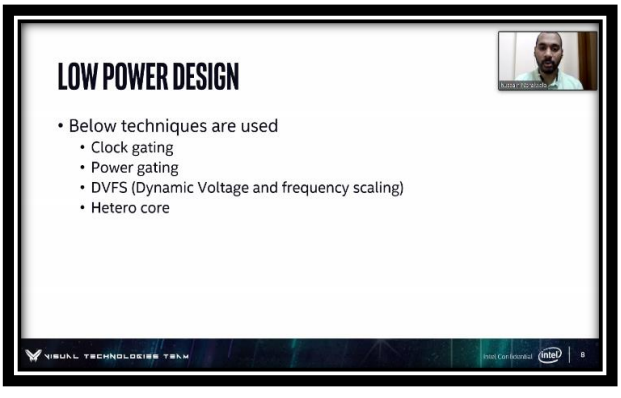












Report Prepared by: Ms. Shubhangi Katariyar (Alumni Representative EXTC Department)

Report Approved by: Ms. Gejo George (Alumni Committee Member EXTC Department)