Module No.	Unit No.	Topics	Hrs.
1.0		**Number Systems and Codes**	**04**
	1.1	Review of Binary, Octal and Hexadecimal Number Systems, their inter-conversion, Binary code, Gray code and BCD code, Binary Arithmetic, Addition, Subtraction using 1's and 2's Complement	04
2.0		**Logic Family and Logic Gates**	**05**
	2.1	Difference between Analog and Digital signals, Logic levels, TTL and CMOS Logic families and their characteristics	03
	2.2	Digital logic gates, Universal gates, Realization using NAND and NOR gates, Boolean Algebra, De Morgan's Theorem	02
3.0		**Combinational Logic Circuits**	**12**
	3.1	SOP and POS representation, K-Map up to four variables and Quine-McClusky method for minimization of logic expressions	04
	3.2	Arithmetic Circuits: Half adder, Full adder, Half Subtractor, Full Subtractor, Carry Look ahead adder and BCD adder, Magnitude Comparator	04
	3.3	Multiplexer and De-Multiplexer: Multiplexer operations, cascading of Multiplexer, Boolean function implementation using MUX, DEMUX and basic gates, Encoder and Decoder	04
4.0		**Sequential Logic Circuits**	**12**
	4.1	Flip flops: RS, JK, Master slave flip flops; T & D flip flops with various triggering methods, Conversion of flip flops, Registers: SISO, SIPO, PISO, PIPO, Universal Shift Register	04
	4.2	Counters: Asynchronous and Synchronous counters with State transition diagram, Up/Down, MOD N, BCD Counter	04
	4.3	Applications of Sequential Circuits: Frequency division, Ring counter, Johnson counter, Introduction to design of Moore and Mealy circuits	04
5.0		**Different Types of Memories and Programmable Logic Devices**	**04**
	5.1	Classification and Characteristics of memory, SRAM, DRAM, ROM, PROM, EPROM and Flash memories	02
	5.2	Introduction: Programmable Logic Devices (PLD), Programmable Logic Array (PLA), Programmable Array Logic (PAL)	02
6.0		**Introduction to VHDL**	**02**
	6.1	Basics of VHDL/Verilog Programming, Design and implementation of adder, subtractor, multiplexer and flip flop using VHDL/Verilog	02
		Total	**39**